ABSTRACT OF THE DISCLOSURE

A method for driving a liquid crystal display device is disclosed. When data clock (DCLK) is not required, the method of driving a liquid crystal display device with low power consumption enables the close loop of the DCLK. That is, after a data transmission (LOAD) signal is triggered and before a data reception (DSTH) signal is triggered, the timing controller forces the DCLK signal to be at a low voltage level, which means the DCLK signal is not outputted, and therefore power saving is achieved.